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| 10/731,714 | 12/09/2003 | Anupama Anlruddha Agashe | TI-36268 | 5466 |

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| EXAMINER | |
|---|---|
| TRIMMINGS, JOHN P | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2138 | |

DATE MAILED: 04/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/731,714 | AGASHE ET AL. | |
| | Examiner | Art Unit | |
| | John P. Trimmings | 2138 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *09 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6-8* is/are rejected.

7)☒ Claim(s) *1-5,7,8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/12/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

Claims 1-8 are presented for examination.

### *Priority*

1. The examiner acknowledges the applicant's claim of priority under 35 USC 119(e)(1) of provisional application No. 60/501,131.

### *Information Disclosure Statement*

2. The examiner has considered the applicant's Information Disclosure Statement dated 1/12/2004.

### *Specification*

3. The disclosure is objected to because of the following informalities:

a. Page 7: beginning at line 7 and ending at line 14, references to "Figure 1" should be corrected to read, "Figures 1a and 1b".

b. Page 7: line 18, "of Figure 2" should be deleted.

c. Page 8: line 23 and 24 should change "Figure 1" to read, "Figure 1a".

d. Page 9: line 13 should be corrected to read, "... mechanism 116 as shown in Figure 1b. ...".

e. Page 14: line 20 should be corrected to read, "... signal $SCAN_{EN}$. ~~NOR~~ XOR gate 308 ...".

f. Page 15: line 22 should be corrected to read, "... signal $TEST_{CLK}$. ~~NOR~~ XOR gate 422 ...".

g. Page 16: line 13 should be corrected to read, "... signal $TEST_{CLK}$. ~~NOR~~ XOR gate 522 ...".

h. Page 16: line 30 should be corrected to read, "... signal $TEST_{CLK}$. ~~NOR~~ XOR gate 622 ...".

i. Page 17: line 11 should be corrected to read, "... signal $TEST_{CLK}$. ~~NOR~~ XOR gates ...".

Appropriate correction is required.

***Claim Objections***

4. Claim 1 is objected to because of the following informalities:

Lines 35 and 36 should be corrected to recite, "... a plurality of test mode select pin inputs, ...".

Line 36 should also be corrected to recite, "... function clock and function enable ..." in order to be consistent with Claim 2.

Lines 37 and 38 recite, "... to generate a control signal ...", but this is not consistent with "a control input" in line 21 of the claim. It would be clearer if lines 37 and 38 were to recite, "... to generate a the control input signal ...".

Line 45 should be corrected to read, "... the simultaneous test mode ~~signals~~ signal ...", to be consistent with the claim.

5. Claim 2 is objected to because of the following informalities:

If "a test clock" (line 3) is the same clock as in Claim 1, the examiner requests that the phrase be corrected to read, "... a the test clock ...".

Line 9 should also be corrected to recite, "...the function enable and ~~clocking~~ clock signals ..." in order to be consistent with Claim 2.

6. Claim 3 is objected to because of the following informalities:

Line 11 should be corrected to read, "... a ~~NOR~~ XOR gate, ...".

7. Claim 4 is objected to because of the following informalities:

Line 21 should be corrected to read, "... a ~~NOR~~ XOR gate, ...".

Line 22 should be corrected to read, "... to the ~~NOR~~ XOR gate; ...".

8. Claim 5 is objected to because of the following informalities:

Line 6 should be corrected to read, "... a plurality of ~~NOR~~ XOR gates, ...".

Line 9 should be corrected to read, "... the plurality of ~~NOR~~ XOR gates ...".

9. Claim 5 is objected to because of the following informalities:

Line 5 should be corrected to read, "... (a) applying a test mode select code ...".

10. Claim 7 is objected to because of the following informalities:

Line 15 should be corrected to read, "... separated by ~~the~~ twice the period ...".

11. Claim 8 is objected to because of the following informalities:

Line 16 should be corrected to read, "... separated by ~~the~~ twice the period ...".

Appropriate correction is required.

***Duplicate Claims, Warning***

12. Applicant is advised that should Claim 7 be found allowable, Claim 8 will be objected to under 37 CFR 1.75 as being a substantial duplicate thereof. When two claims in an application are duplicates or else are so close in content that they both cover the same thing, despite a slight difference in wording, it is proper after allowing one claim to object to the other as being a substantial duplicate of the allowed claim. See MPEP § 706.03(k).

***Claim Rejections - 35 USC § 112***

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

13. Claim 6 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Step (b) cites simultaneously capturing all scan chain groups corresponding to one of the test clock rate. This limitation is indefinite because the step is placed inside a loop of steps that scan in to each scan group separately, and so the

examiner is not sure if the applicant wants to capture all groups until all of the groups are scanned.

Also, the limitation clocks the capture at the test clock rate, which is contrary to the test protocol of at speed testing, and so the claim is indefinite.

14. Claim 7 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Step (c) cites simultaneously capturing all scan chain groups corresponding to one of the test clock rate. This limitation is indefinite because the step, which captures all scan-chain groups, is placed inside a loop of steps that scan in to each scan group separately, and so the examiner is not sure if the applicant wants to capture all groups until all of the groups are scanned.

Also, the limitation clocks the capture at the test clock rate (lines 15 and 16), which is contrary to the test protocol described in the Specification.

Also, line 15 of the claim applies "two capture pulses", which is also contrary to the Specification for stuck at fault testing.

15. Claim 8 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Step (c) cites simultaneously capturing all scan chain groups corresponding to one of the test clock rate. This limitation is indefinite because the step, which captures all scan-chain groups, is placed inside a loop of steps that scan in to

each scan group separately, and so the examiner is not sure if the applicant wants to capture all groups until all of the groups are scanned.

Also, the limitation clocks the capture at the test clock rate (lines 16 and 17), which is contrary to the test protocol described in the Specification.

Also, line 16 of the claim applies "two capture pulses separated by twice the period ...", which is also contrary to the Specification for at speed testing.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

16. Claims 6-8 are rejected under 35 U.S.C. 102(e) as being anticipated by Wang et al. (herein Wang), U.S. Patent No. 7007213.

As per Claim 6:

A method for testing an integrated circuit chip having at least two clock domains at respective domain test clock rates corresponding to at least two scan chain groups, using a very low cost test (VLCT) platform-Automatic Test Pattern Generator (see Abstract), comprising: (a) clocking a test stimulus input data into each scan chain of each said clock domain sequentially (see FIG.23) by clocking the test stimulus input

data into one scan chain and disabling the clocks of the other respective scan chain groups to hold these other respective scan chain groups static (example, FIG.23 CK1 at time 2301 is on, all others off), clocking said test stimulus input data at a shift clock rate derived from at least one of said scan chain clock domains (see FIG.7 and FIG.9); (b) capturing on all scan chain groups resultant data simultaneously at a predetermined frequency corresponding to one of the plurality of scan chain groups domain test clock rate (example, FIG.5 CK1 and CK3); (c) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency (see FIG.8 where each domain stores into a MISR); (d) repeating steps (a)-(c) at a corresponding frequency for each of the at least two scan chain groups (example, FIG.23 CK1 goes to CK2, to CK3 ...).

As per Claims 7 and 8:

A method for fault testing an integrated circuit chip having at least two clock domains at respective domain test clock rates corresponding to at least two scan chain groups, using a very low cost test (VLCT) platform for a full device scan Automatic Test Pattern Generator (see Abstract), comprising: (a) applying test mode select code signal to a plurality of test mode select pins (FIG.2 204, 205) of a clock control mechanism (FIG.2) for controlling the shift scan inputs of the at least two scan chain groups; (b) shifting a test stimulus input data into each scan chain of each said clock domain sequentially (see FIG.23) by shifting the test stimulus input data into one scan chain and disabling the clocks of the other respective scan chain groups to hold these other respective scan chain groups static (example, FIG.23 CK1 at time 2301 is on, all others

off), shifting said test stimulus input data at a shift clock rate derived from at least one of said scan chain clock domains (see FIG.7 and FIG.9); (c) capturing on all scan chain groups resultant data simultaneously at a predetermined frequency corresponding to one of the plurality of scan chain groups domain test clock rate by applying two capture pulses separated by the twice the period of the corresponding domain test clock rate (example, FIG.5 CK1 and CK3); (d) storing resultant data from one of the plurality of scan chain groups that corresponds with the predetermined frequency (see FIG.8 where each domain stores into a MISR); (e) repeating steps (a)-(d) at a corresponding frequency for each of the at least two scan chain groups (example, FIG.23 CK1 goes to CK2, to CK3 ...).

***Allowable Subject Matter***

17. Claims 1-5 are allowed. The following is an examiner's statement of reasons for allowance: The reference Wang, combined with the pertinent art of Crouch, disclose a scan test design comprising scan groups driven by different clock domains, a demultiplexer for receiving the test input and applying a vector to a scan chain group under control of a domain clock, a 2nd multiplexer to receive functional output data, a controlling demultiplexer to select output data, a clock controller to control input scanning separately, and capture clocking being executed in parallel. However, the references fail to teach, disclose or suggest features claimed in the present application, in particular, the test clock enables testing of each group, a 1st multiplexer unit located

between the demultiplexer and each scan group, with the design having a plurality of test mode select pins. Therefore, the claims 1-5 are allowed.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

18. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Crouch et al. (herein Crouch), U.S. Patent No. 5592493.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John P. Trimmings whose telephone number is (571) 272-3830. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

John P Trimmings
Examiner
Art Unit 2138

jpt

GUY LAMARRE
PRIMARY EXAMINER